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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/663,777	09/18/2000	Darren Kerr	112025-0197	4077

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CESARI AND MCKENNA, LLP
88 BLACK FALCON AVENUE
BOSTON, MA 02210

EXAMINER	
STEVENS, ROBERTA A	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/663,777	KERR ET AL.	
	Examiner	Art Unit	
	Roberta A Stevens	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10-08-2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9,10 and 20* is/are allowed.

6)☒ Claim(s) *1-8, 11-19, 21-29, 31-38 and 40-48* is/are rejected.

7)☒ Claim(s) *30 and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. Claims 1, 2, 4-7, 11-16, 18 and 21-23, 25-28, 31, 32, 34-37, 40, 41, 43 and 44 are rejected under 35 U.S.C. 102(e) as being anticipated by Wu (U.S. 6151644).

2. Regarding claim 1, Wu teaches (col. 1, line 58 – col. 2, line 14) a method for striping packets across pipelines of processing engine within a network switch, the processing engine having a plurality of processors arrayed as pipeline rows and columns embedded between input (20) and output (22) buffer (fig. 2), each pipeline row including a context memory, comprising: organizing the context memory as a plurality of window buffers of a defined size (col.1 lines 58-61); apportioning each packet into contexts corresponding to the defined size associated with each window buffer (col. 1 lines 61-66); and correlating each context with a relative position within the packet to thereby facilitate reassembly of the packet at the output buffer, while obviating out-of-order issues involving the contexts of the packet (col. 1 line 66- col. 2, line 14).

3. Regarding claims 2, 12, 23, 32 and 41, Wu teaches (figure 2) organizing the processors and context memory of each pipeline row as a cluster.

4. Regarding claims 4, 13, 18, 25, 34 and 43, Wu teaches (col. 5, lines 10-28) providing a program counter entry point function to indicate the relative position of each context within the packet.

5. Regarding claims 5, 14, 26, 35 and 44, Wu teaches (col. 5, lines 29-54) the relative position comprises one of a beginning, middle and end context of the packet.

6. Regarding claims 6, 27, 36 and 45, Wu teaches (col. 5, lines 54 – col. 6) processing the context at a source processor of the cluster; communicating an intermediate result relating to processing of the context to a destination processor of a neighboring cluster.

7. Regarding claims 7, 15, 28, 37 and 46, Wu teaches (fig. 2) providing an intercolumn communication mechanism configured to forward the intermediate result from the source processor.

8. Regarding claim 11, Wu teaches (col. 1, line 58 – col. 2, line 14) a system for striping packets across pipelines of a processing engine within a network switch, the processing engine having a plurality of processors arrayed as pipeline rows and columns embedded between input and output buffers (fig. 2), comprising: a context memory within each pipeline row, organized as a plurality of window buffers of a defined size (col.1 lines 58-61); a segmentation unit adapted to apportion each packet into contexts for processing, corresponding to the defined size associated with each window buffer (col. 1, lines 61-66); and a mapping mechanism configured to correlate each context with a relative position within the packet to thereby facilitate reassembly of the packet at the output buffer while obviating out of order issues involving the context of the packet (col. 1 line 66- col. 2, line 14).

9. Regarding claim 16, Wu teaches (col. 1, line 58 – col. 2, line 14) a computer readable medium containing program instructions for striping packets across pipelines of processing engine within a network switch, the processing engine having a plurality of processors arrayed as pipeline rows and columns embedded between input output buffer (fig. 2) each pipeline row including a context memory, comprising: organizing the context memory as a plurality of window buffers of a defined size (col.1 lines 58-61); apportioning each packet into contexts corresponding to the defined size associated with each window buffer (col. 1, lines 61-66); and correlating each context with a relative position within the packet to thereby facilitate reassembly of the packet at the output buffer, while obviating out-of-order issues involving the contexts of the packet (col. 1 line 66- col. 2, line 14).

10. Regarding claim 21, Wu teaches (col. 1, line 58 – col. 2, line 14) an electromagnetic signal propagation on a computer network carrying instructions for striping packets across pipelines of processing engine within a network switch, the processing engine having a plurality of processors arrayed as pipeline rows and columns embedded between input output buffer (fig. 2) each pipeline row including a context memory, the processors and context memory organized as a cluster, comprising: organizing the context memory as a plurality of window buffers of a defined size (col.1 lines 58-61); apportioning each packet into contexts corresponding to the defined size associated with each window buffer (col. 1, lines 61-66); and correlating each context with a relative position within the packet to thereby facilitate reassembly of the packet at the output buffer, while obviating out-of-order issues involving the contexts of the packet (col. 1 line 66- col. 2, line 14).

11. Regarding claim 22, Wu teaches (col. 1, line 58 – col. 2, line 14) a method for operating a network switch, comprising: arraying a plurality of processors as a plurality of rows (fig. 2A-3F), a row forming a pipeline row, the pipeline rows arrayed between an input buffer (20) and an output buffer (22); (fig. 2), comprising: including a context memory in each pipeline row, organizing the context memory as a plurality of window buffers of a defined size (col.1 lines 58-61); apportioning by the input buffer, each packet into contexts, corresponding to the defined size associated with each window buffer (col. 1, lines 61-66); and correlating each context with a relative position within the packet to thereby facilitate reassembly of the packet at the output buffer, to facilitate striping packets across a plurality of the pipelines (col. 1 line 66- col. 2, line 14).

12. Regarding claim 31, Wu teaches (col. 1, line 58 – col. 2, line 14) a processing engine within a network switch, comprising: means for arraying a plurality of processors as a plurality of rows (fig. 2A-3F), a row forming a pipeline row, the pipeline rows arrayed between an input buffer (20) and an output buffer (22); (fig. 2), comprising: means for including a context memory in each pipeline row; means for organizing the context memory as a plurality of window buffers of a defined size (col.1 lines 58-61); means for apportioning by the input buffer, each packet into contexts, corresponding to the defined size associated with each window buffer (col. 1, lines 61-66); and means for correlating each context with a relative position within the packet to thereby facilitate reassembly of the packet at the output buffer, to facilitate striping packets across a plurality of the pipelines (col. 1 line 66- col. 2, line 14).

13. Regarding claim 40, Wu teaches (col. 1, line 58 – col. 2, line 14) a processing engine within a network switch, comprising: a plurality of processors arrayed as a plurality of rows (fig. 2A-3F), a row forming a pipeline row, the pipeline rows arrayed between an input buffer (20) and an output buffer (22); (fig. 2), a context memory included in each pipeline row; the context memory organized as a plurality of window buffers of a defined size (col.1 lines 58-61); the input buffer apportioning each packet into contexts corresponding to the defined size associated with each window buffer (col. 1 lines 61-66); and a processor of the plurality of processors to correlate each context with a relative position within the packet to thereby facilitate reassembly of the packet at the output buffer, thereby facilitating striping packets across the plurality of pipelines (col. 1 line 66- col. 2, line 14).

Claim Rejections - 35 USC § 103

14. . Claims 3, 8, 17, 19, 24, 29, 33, 38, 42, 47 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu in view of Sindhu.

15. Wu teaches (figure 2) sequentially passing the contexts to the clusters; and storing the contexts in appropriate window buffers of the context memories.

16. Wu does not teach segmenting the packets into fixed sized contexts at the input buffer.

17. Sindhu teaches (col. 6, lines 58-65) dividing the received packets into fixed length cells. It would have been obvious to one of ordinary skill in this art to adapt to Wu's system Sindhu's concept of dividing the packets into fixed length cells to make the system more efficient.

Allowable Subject Matter

18. Claims 9, 10 and 20 are allowed.

19. Claims 30 and 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

20. Applicant's arguments filed October 8, 2004 have been fully considered but they are not persuasive. Applicant argues that Wu does not teach striping packets across pipelines of processing engine within a network switch, the processing engine having a plurality of processors arrayed as pipeline rows and columns embedded between input output buffer, however, Wu teaches the processing engine having a plurality of processors arrayed as pipeline

rows and columns (fig. 3a-3F) embedded between input (20) and output (22) buffers (fig. 2). Applicant also argues that Wu does not teach correlating each context with a relative position within the packet to thereby facilitate reassembly of the packet at the output buffer, while obviating out-of-order issues involving the contexts of the packet. Applicant is directed to Wu (col. 1 line 66- col. 2, line 14) where it is explained that the order of the packet buffers, containing the segments of each packet, is maintained so that the packet can be properly reassembled.

Conclusion

21. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

22. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberta A Stevens whose telephone number is 571-272-3161. The examiner can normally be reached on M-F 9:00am-5:30pm.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Roberta A Stevens
Examiner
Art Unit 2665

STEVEN NGUYEN
PRIMARY EXAMINER